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Published:
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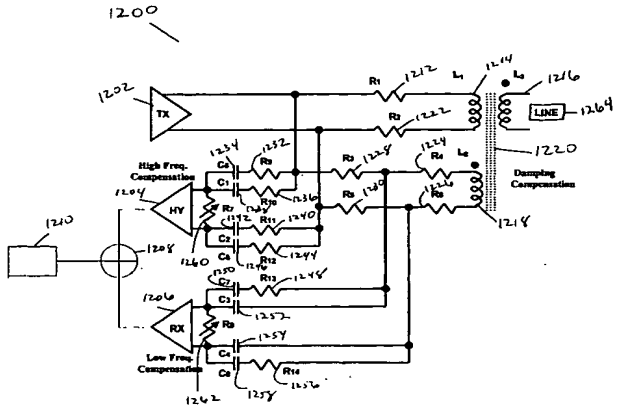
— *with amended claims*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD AND SYSTEM FOR PROVIDING AN ANALOG FRONT END FOR MULTILINE TRANSMISSION IN COMMUNICATION SYSTEMS



(57) Abstract: A method and system for providing an analog front end for multiline transmission in communications systems are described. A transceiver circuit (1100) is configured to reduce line noise by providing a coupled transmitter (1106), receiver (1106), prebalance circuit (1110), and transformer (1220) further coupled to a communication line (1264) external to the transceiver circuit. A hybrid (HY) input stage (1204) coupled to the prebalance circuit provides high frequency compensation by including a first high pass circuit coupled to the HY stage inputs, wherein the high pass circuit includes two parallel passes, each with a capacitor (C1,C5) in series with a resistor (R9,R10). A receiver input stage (RX) (RX) (1206) further coupled to the prebalance circuit provides low frequency compensation by including a second high pass circuit coupled to the RX stage inputs, wherein the high pass circuit includes two parallel passes, one with a capacitor (C3) and one with a capacitor (C7) in series with a resistor (R13). Lastly, a summing junction (1208) coupled to the HY stage (1204) and RX stage (1206) subtracts the HY stage output from the RX stage output providing a filtered incoming analog signal for post processing.

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CLAIMS

What is claimed is:

1. A transceiver circuit configured to reduce line noise comprising:
   a transmitter and a receiver coupled to a prebalance circuit;
   a transformer further coupled to the prebalance circuit, the transformer having a first coil and a second coil coupled to the transceiver circuit and a third coil coupled to a communication line external to the transceiver circuit;
   a hybrid (HY) input stage coupled to the prebalance circuit;
   a first high pass circuit coupled to the HY stage inputs, the high pass circuit for high frequency compensation including two parallel passes, each with a capacitor in series with a resistor;
   a receiver input stage (RX) further coupled to the prebalance circuit;
   a second high pass circuit coupled to the RX stage inputs, the high pass circuit for low frequency compensation including two parallel passes, one with a capacitor and one with a capacitor in series with a resistor; and
   a summing junction coupled to the HY stage and RX stage, the summing junction configured to subtract the HY stage output from the RX stage output.

AMENDED CLAIMS
[received by the International Bureau on 12 November 2003 (12.11.03);
original claims 1 replaced by amended claims 1-39 (6 pages)]

1. A method comprising:

receiving an echo signal at a transceiver, wherein the transceiver includes an Analog Digital Converter (ADC) and Digital-to-Analog Converter (DAC); and

reducing the echo signal with an echo rejecter at an input of the ADC, wherein the echo rejecter has an analog portion and a digital portion.

2. The method of claim 1, further comprising minimizing any loss of ADC resolution with a data signal associated with the echo signal.

3. The method of claim 1, wherein the echo signal includes a transmitter noise signal.

4. The method of claim 1, wherein the transceiver includes an analog front end (AFE), comprising:

an hybrid input stage;
a prebalance circuit;
the echo rejecter;
hybrid inputs;
receiver inputs;
transmitter outputs;
a high-pass filter circuit; and
a low-pass filter circuit.

5. The method of claim 4, wherein the AFE implements echo rejection across an entire usable frequency band

6. The method of claim 3, further comprising lowering the transmitter noise signal and removing the echo signal completely with the digital portion of the echo rejecter.

7. The method of claim 6, further comprising designing the high-pass filter circuit with a transmission line model; and designing the low-pass filter circuit with the transmission line model.

8. The method of claim 6, further comprising using the transceiver in a multiline communications system, wherein the multiline communications system treats multiple twisted copper pairs as a single multiline communications channel.

9. A system comprising:

means for receiving an echo signal at a transceiver, wherein the transceiver includes an Analog Digital Converter (ADC) and Digital-to-Analog Converter (DAC); and

means for reducing the echo signal with an echo rejecter at an input of the ADC,

wherein the echo rejecter has an analog portion and a digital portion.

10. The system of claim 9, further comprising means for minimizing any loss of ADC resolution with a data signal associated with the echo signal.

11. The system of claim 9, wherein the echo signal includes a transmitter noise signal.

12. The system of claim 9, wherein the transceiver includes an analog front end (AFE), comprising:

an hybrid input stage;

a prebalance circuit;

hybrid inputs;

receiver inputs;

transmitter outputs;

a high-pass filter circuit; and

a low-pass filter circuit.

13. The system of claim 12, wherein the AFE implements echo rejection across an entire usable frequency band.

14. The system of claim 11, further comprising means for lowering the transmitter noise signal and removing the echo signal completely with the digital portion of the echo rejecter.

15. The system of claim 14, further comprising means for designing the high-pass filter circuit with a transmission line model; and means for designing the low-pass filter circuit with the transmission line model.

16. The system of claim 14, further comprising means for using the transceiver in a multiline communications system, wherein the multiline communications system treats multiple twisted copper pairs as a single multiline communications channel.

17. An apparatus, comprising:
a receiver;
receiver inputs coupled to the receiver;
a transmitter coupled to the receiver;
transmitter outputs coupled to the transmitter; and
an echo rejecter coupled to the receiver and the transmitter,
wherein the echo rejecter has an analog portion and a digital portion.

18. The apparatus of claim 17, wherein the echo rejecter further comprises:
an hybrid input stage having hybrid inputs; and
a prebalance circuit coupled to the hybrid input stage,
wherein the receiver inputs are coupled to the prebalance circuit.

19. The apparatus of claim 18, wherein the hybrid input stage is coupled to a high-frequency compensation circuit.

20. The apparatus of claim 19, wherein the high-frequency compensation circuit comprises a first high-pass filter circuit, wherein the first high-pass filter circuit includes a first parallel pass and second parallel pass, the first parallel pass including a first capacitor and the second parallel pass including a second capacitor in series with a resistor.

21. The apparatus of claim 18, wherein the receiver inputs are coupled to a low-frequency compensation circuit.

22. The apparatus of claim 21, wherein the low-frequency compensation circuit comprises: a second high-pass filter circuit, wherein the second high-pass filter circuit includes a first parallel pass and second parallel pass, the first parallel pass including a first capacitor and the second parallel pass including a second capacitor in series with a resistor.

23. The apparatus of claim 20, wherein the receiver inputs are coupled to a low-frequency compensation circuit.

24. The apparatus of claim 23, wherein the low-frequency compensation circuit comprises: a second high-pass filter circuit, wherein the second high-pass filter circuit includes a third parallel pass and fourth parallel pass, the third parallel pass including a third capacitor and the fourth parallel pass including a fourth capacitor in series with a second resistor.

25. The apparatus of claim 24, further comprising a summing junction coupled to the hybrid input stage and receiver input stage, wherein

the high-frequency and low-frequency compensation circuits are coupled to the summing junction, and

the summing junction is configured to subtract a hybrid stage output from a receiver output.

26. The apparatus of claim 25, further comprising an analog to digital converter coupled to the summing junction.

27. The apparatus of claim 25, further comprising a digital to analog converter coupled to the transmitter.

28. A system, comprising:

a communications line; and

a transceiver coupled to the communications line, wherein the transceiver comprises

a receiver;

receiver inputs coupled to the receiver;

a transmitter coupled to the receiver;

transmitter outputs coupled to the transmitter; and

an echo rejecter coupled to the receiver and the transmitter,

wherein the echo rejecter has an analog portion and a digital portion.

29. The system of claim 28, wherein the echo rejecter further comprises: an hybrid input stage having hybrid inputs; and a prebalance circuit coupled to the hybrid input stage, wherein the receiver inputs are coupled to the prebalance circuit.

30. The system of claim 29, wherein the communications line is a single multiline communications channel having multiple twisted copper pairs, and coordinates physical-layer signals across multiple transmitters and across multiple receivers.

31. The system of claim 29, wherein the hybrid input stage is coupled to a high-frequency compensation circuit.

32. The system of claim 31, wherein the high-frequency compensation circuit comprises a first high-pass filter circuit, wherein the first high-pass filter circuit includes a first parallel pass and second parallel pass, the first parallel pass including a first capacitor and the second parallel pass including a second capacitor in series with a resistor.

33. The system of claim 29, wherein the receiver inputs are coupled to a low-frequency compensation circuit.

34. The system of claim 33, wherein the low-frequency compensation circuit comprises: a second high-pass filter circuit, wherein the second high-pass filter circuit includes a first parallel pass and second parallel pass, the first parallel pass including a first capacitor and the second parallel pass including a second capacitor in series with a resistor.

35. The system of claim 32, wherein the receiver inputs are coupled to a low-frequency compensation circuit.

36. The system of claim 35, wherein the low-frequency compensation circuit comprises: a second high-pass filter circuit, wherein the second high-pass filter circuit includes a third parallel pass and fourth parallel pass, the third parallel pass including a third capacitor and the fourth parallel pass including a fourth capacitor in series with a second resistor.

37. The system of claim 36, further comprising a summing junction coupled to the hybrid input stage and receiver input stage, wherein

the high-frequency and low-frequency compensation circuits are coupled to the summing junction, and

the summing junction is configured to subtract a hybrid stage output from a receiver output.

38. The system of claim 37, further comprising an analog to digital converter coupled to the summing junction.

39. The system of claim 37, further comprising a digital to analog converter coupled to the transmitter.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US03/18127

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : H04B 7/005, 3/20; H04M 1/00, 9/08; H04L 5/16
US CL : 370/278, 286, 289, 290; 379/390.04, 406.05, 402; 375/222

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 370/278, 286, 289, 290; 379/390.04, 406.05, 402; 375/222

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
Please See Continuation Sheet

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A, P	US 6,421,377 B1 (LANGBERG et al.) 16 July 2002. See entire document.	1
A, P	US 6,442,195 B1 (LIU et al.) 27 August 2002. See entire document.	1
A	US 5,917,809 A (RIBNER et at.) 29 June 1999. See entire document.	1

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

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INTERNATIONAL SEARCH REPORT

Continuation of Item 4 of the first sheet:
METHOD AND SYSTEM PROVIDING ANALOG FRONT END FOR MULTILINE TRANSMISSION

Continuation of B. FIELDS SEARCHED Item 3:
EAST
echo canceler, hybrid, transformer, modem ,